

FIG. 1 is a schematic diagram of a system 100 in accordance with one embodiment of the present invention. The system 100 includes a host 110 and a plurality of devices 121, 122, 123, and 124. The host 110 is connected to the devices 121, 122, 123, and 124 via a network 115. The network 115 is a bus network, and the devices 121, 122, 123, and 124 are connected to the network 115 via network interfaces 121F, 122F, 123F, and 124F, respectively. The host 110 includes a processor 116 and a memory 117. The processor 116 is connected to the memory 117 and the network 115. The memory 117 is connected to the processor 116 and the network 115. The devices 121, 122, 123, and 124 are connected to the network 115 via network interfaces 121F, 122F, 123F, and 124F, respectively. The network 115 is a bus network, and the devices 121, 122, 123, and 124 are connected to the network 115 via network interfaces 121F, 122F, 123F, and 124F, respectively.

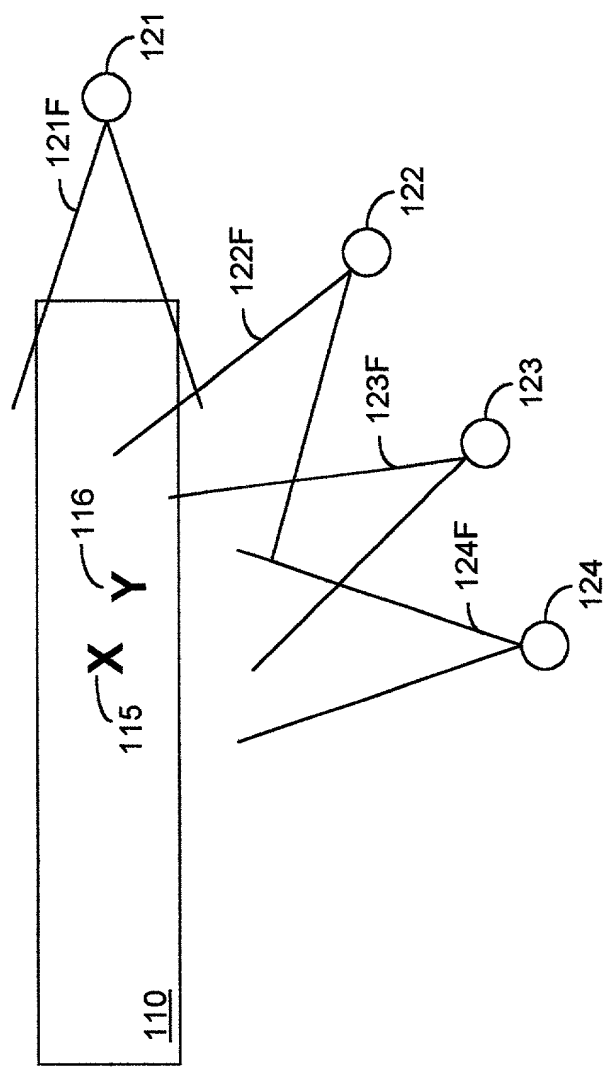


Figure 1
(PRIOR ART)

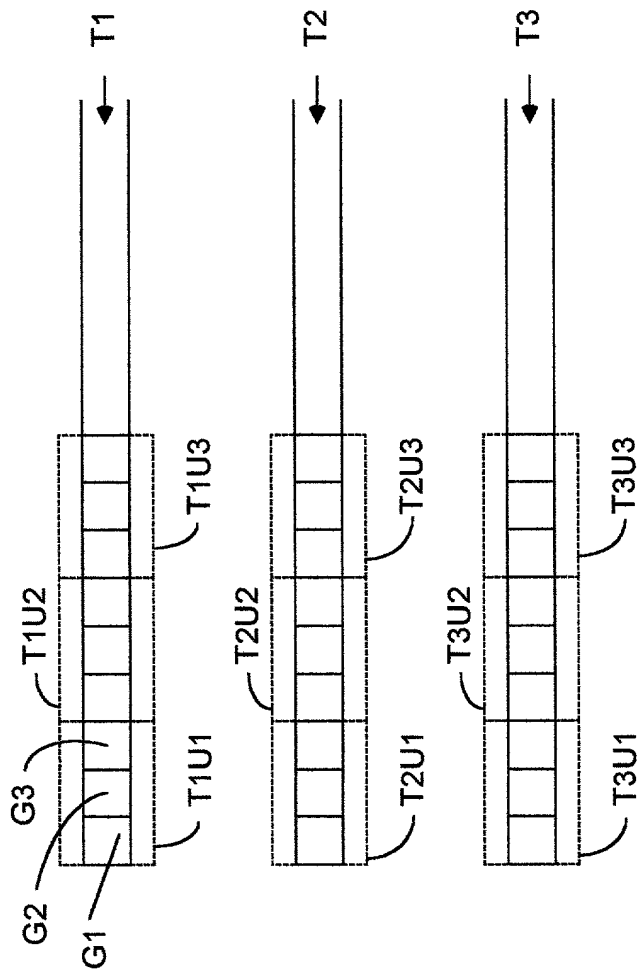


Figure 2A
(PRIOR ART)

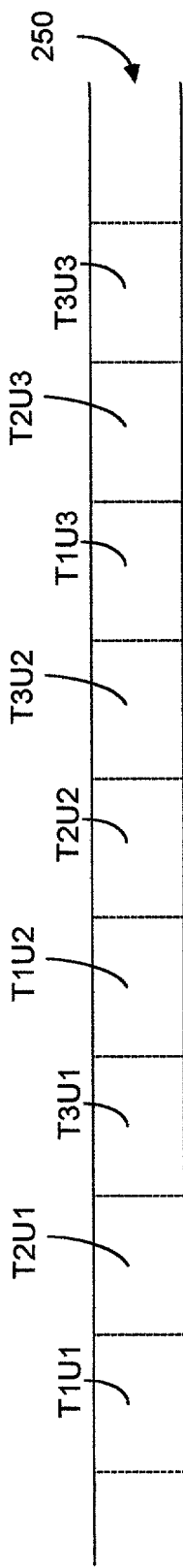


Figure 2B
(PRIOR ART)

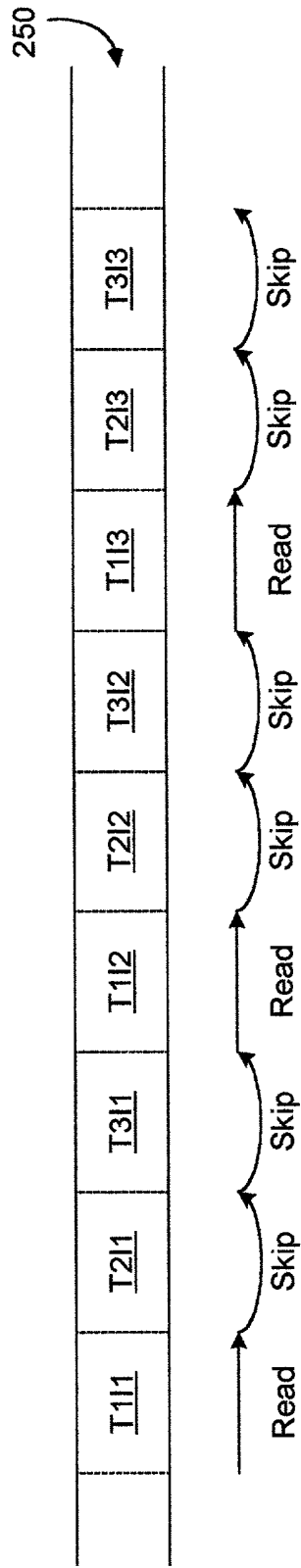


Figure 3A
(PRIOR ART)

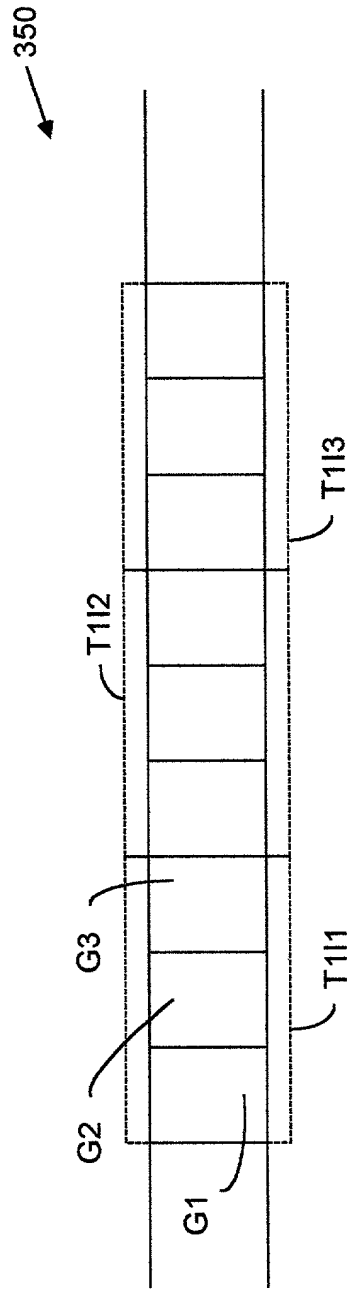


Figure 3B
(PRIOR ART)

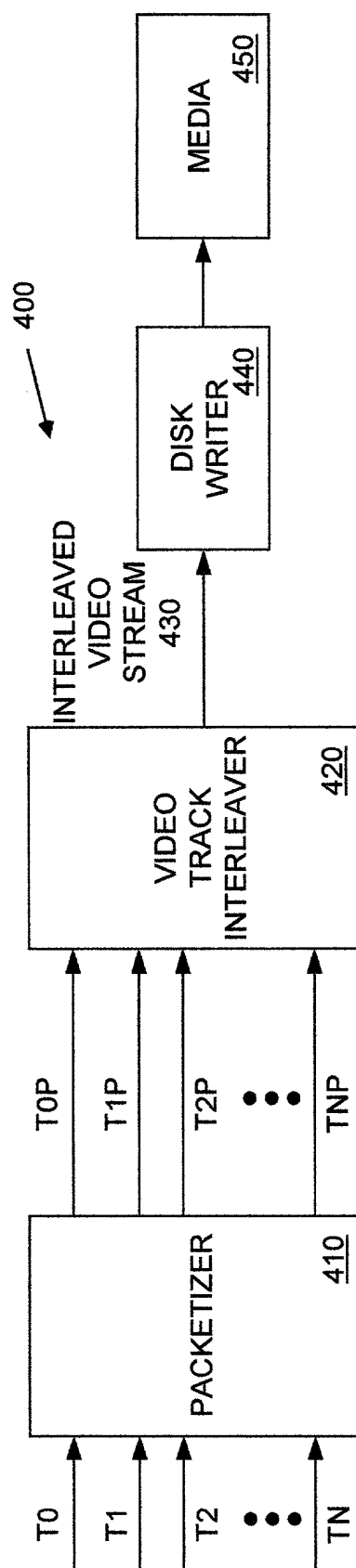


Figure 4A

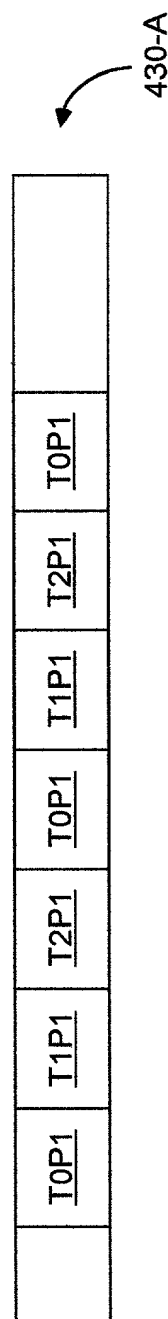


Figure 4B

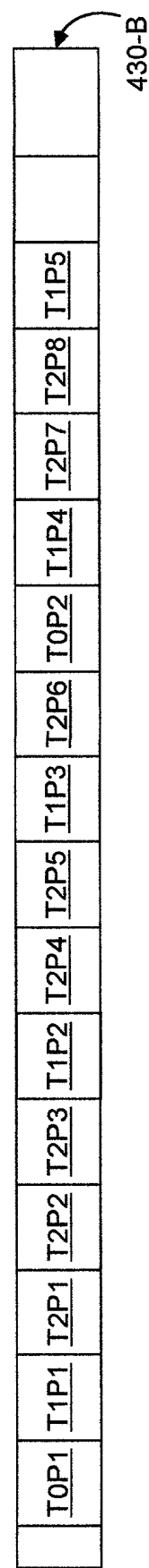


Figure 4C

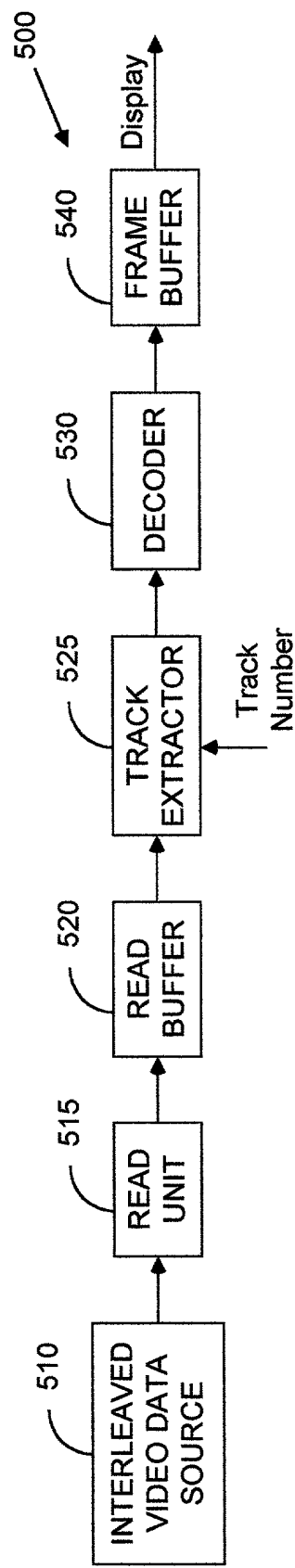


Figure 5A

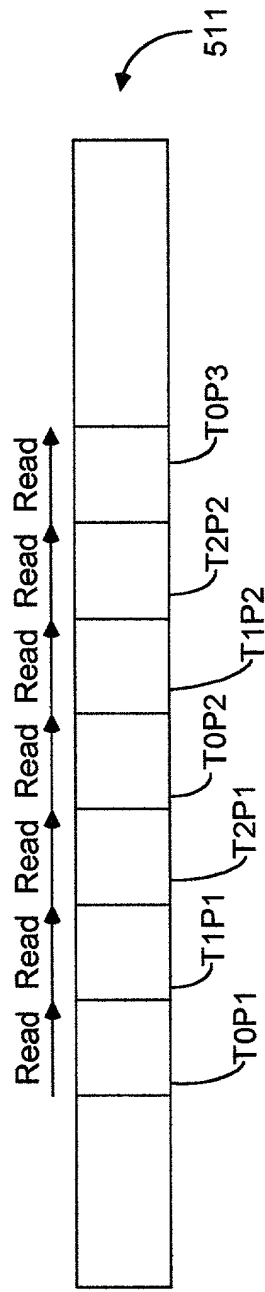


Figure 5B

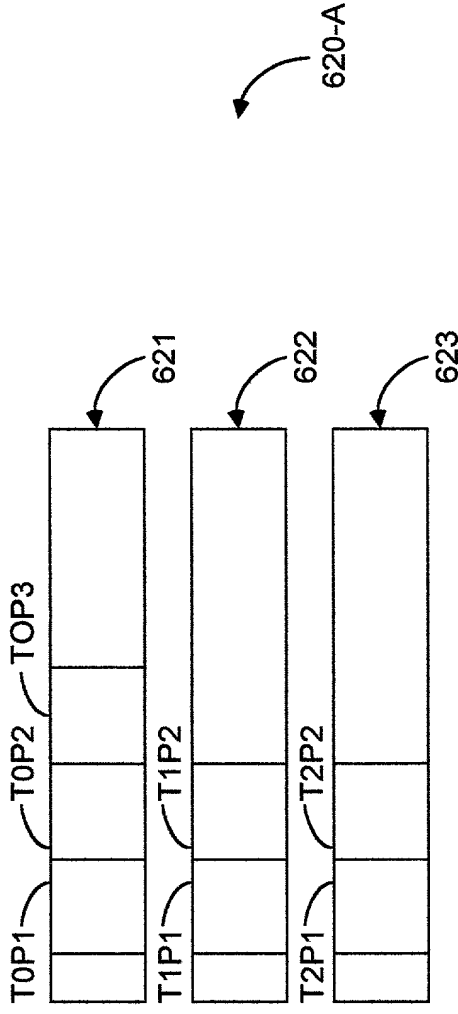


Figure 6A

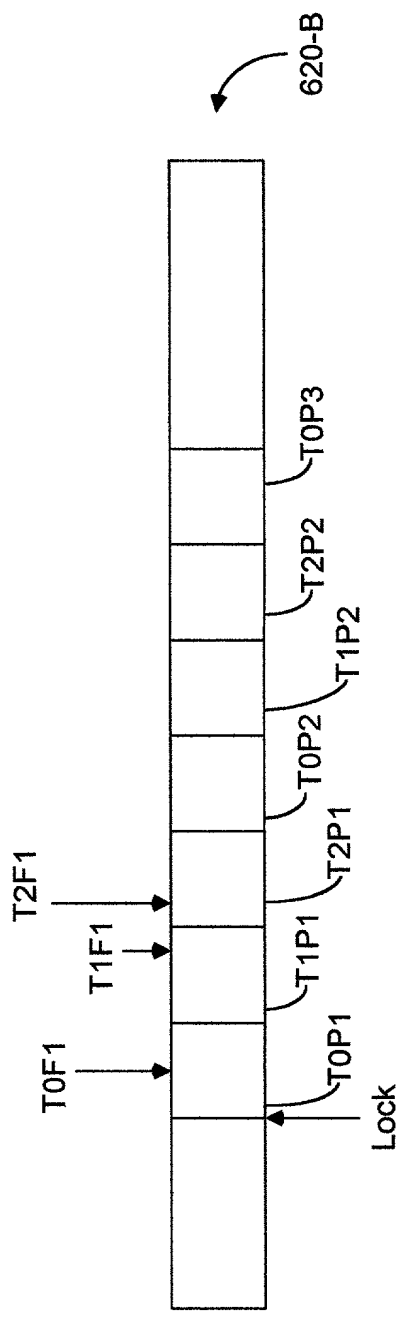


Figure 6B

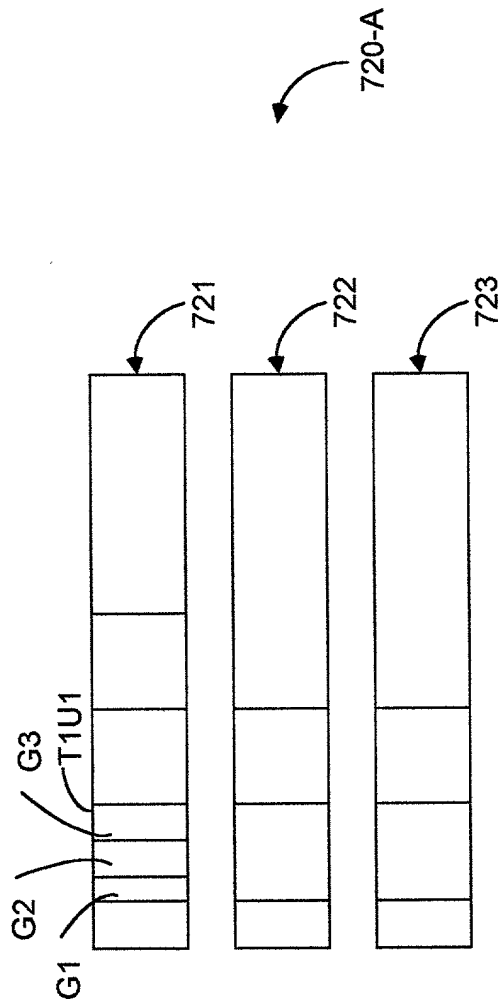


Figure 7A

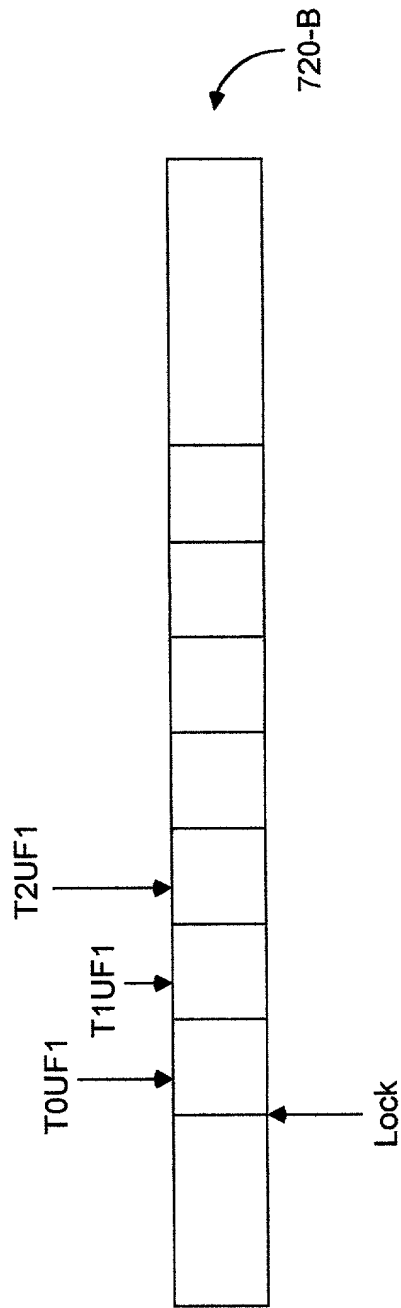


Figure 7B